

摘要

二十世纪九十年代,数字视频技术被广泛应用于通信、计算机、广播电视等领域,带来了电视会议、可视电话、数字电视以及媒体存储等一系列应用,推动了以 MPEG-2 为代表的新一代信源编码标准的产生。进入新世纪以来,随着音视频编解码技术的进步和超大规模集成电路集成度、计算速度的提高,信源编码标准迎来了更新换代的历史性机遇。在这个背景下,以 H.264/AVC、AVS 为代表的第二代信源编码标准出现了。H.264/AVC 是一个高效的视频编码标准,是由国际电信联盟和国际标准化组织运动图像专家组组成的“联合视频组”制订的。AVS 标准是我国具有自主知识产权的信源编码标准,其视频标准的主要应用对象是标准清晰度/高清晰度电视。在标准清晰度/高清晰度序列上,AVS 视频标准的编码效率与 H.264/AVC 相当,是 MPEG-2 的 2~3 倍。

2006 年 2 月,AVS 视频标准已经正式被批准为国家标准,进入了产业化推广的阶段。作为 AVS 编码标准产业链上的重要一环,AVS 标准清晰度/高清晰度视频编解码芯片的研发对于 AVS 编码标准的推广起着重要的推动作用。本文对 AVS 标准清晰度/高清晰度视频编解码芯片中的三个关键部件——运动估计模块、环路滤波模块和变长解码模块的体系结构进行了深入的研究和探讨,下面给出一个简要的介绍:

1. 运动估计是 AVS 视频编码芯片中的关键部件,计算量占整个编码器的 60%~90% 以上。特别是,AVS 视频标准中采用了多参考帧、变块大小的运动估计,高效的 B 帧编码模式等技术,在提高了编码效率的同时,也大大增加了计算的复杂度。基于算法—结构联合设计的思想,本文中提出了一个面向硬件实现的快速整数精度运动估计算法,并给出了相应的 VLSI 实现。实验结果表明该算法具有和 AVS 视频参考软件相当的编码效率,并且相应的 VLSI 结构可以在较低的时钟频率下,支持标清视频在较大搜索范围内的实时处理;

2. 环路滤波是 AVS 视频编解码芯片都要用到的关键部件,其结构设计的关键在于如何增加计算的并行度,同时降低对存储器带宽的占用。本文提出了两种环路滤波处理顺序及其相应的 VLSI 实现。利用了分开存储相邻块数据的组织策略和一个可配置的行列转换阵列,两种 VLSI 结构都可以满足高清视频序列的实时滤波。这两种结构在面积和速度上各占优势;

3. 变长解码器是 AVS 视频解码芯片中的关键部件,其处理速度直接影响到解码操作的实时性。本文提出的多用途变长解码加速器能够支持 AVS 视频标准中采用的所有熵编码算法。该结构根据嵌入式处理器的指令,完成典型 AVS 高清视频序列的实时熵解码,并包含进行起始码检测和丢弃填充位操作的预处理模块。

本文对上述三个 AVS 视频编解码芯片关键部件体系结构的研究,有助于 AVS 标清/高清视频编解码芯片的开发,并且有助于 AVS 标准的产业化。

关键词 AVS 视频编解码器;超大规模集成电路;运动估计;环路滤波;变长解码器

Abstract

In the 1990's, digital video technology was widely used in the field of communication, computer, TV broadcast and so on. The related applications of digital video technology, such as TV conference, videophone, digital TV and media storage, have pushed the production of the first generation source coding standards, such as MPEG-2. In the new century, depending on the improvement of audio-visual coding technique and the enhancement of integration degree and processing speed of VLSI implementation, source coding standards get the best chance of being upgraded. Under these conditions, the second generation and high efficient source coding standards are emerging, such as H.264/AVC and AVS standard. H.264/AVC is an advanced video coding standard, which is developed by Joint Video Team of ITU and ISO/MPEG. AVS standard is a source coding standard of China with independent intellectual properties, whose applications are mainly SDTV and HDTV. For SDTV and HDTV sequences, the coding efficiency of AVS video standard is similar to that of H.264/AVC, and is about 2 or 3 times of that of MPEG-2.

AVS video standard has been approved as Chinese national standard in Feb. 2006. Now the new standard is at the stage of industrialization. In the industrial chain of AVS standard, the research and design for AVS SDTV and/or HDTV codec chip is one of the most important parts. The architectures of three key units in AVS SDTV and/or HDTV codec chip, which is motion estimation unit, loop filter and variable length decoder, are carefully studied and discussed in this dissertation. The brief descriptions of these architectures are as follows.

1. Motion estimation is a key unit of AVS video encoder chip, which takes about 60%~90% computational load of the whole encoder. Especially, AVS video standard adopts some new features such as multiple-reference-frames motion estimation, variable-block-size motion estimation, and high efficient coding modes for B pictures. Although these new features improve the coding efficiency, the computational complexity is greatly increased. Based on the idea of algorithmic and architectural co-design, one hardware-oriented fast integer motion estimation algorithm and its VLSI implementation are proposed in this dissertation. The experimental results show that coding efficiency of the proposed algorithm is similar to that of AVS video reference software, and under the lower working frequency, the VLSI architecture can support real-time processing for SDTV video in the larger search area.

2. Loop filter is a key unit of both AVS video encoder and decoder chips, whose architecture design is focused on increasing computational concurrency and decreasing bandwidth requirement of memory access. Two kinds of loop filter processing order and their VLSI implementations are proposed in this dissertation. Taking the advantages of column-separated SRAM organization and a configurable matrix transposer, the two VLSI architectures can both support the real-time loop filtering for HDTV video sequences. The two architectures have their advantage of either area or speed respectively.

3. Variable length code decoder is a key unit of AVS video decoder chip, whose processing speed directly affects real-time processing of the whole chip. A versatile variable length code decoder is proposed in this dissertation, which can support all types of entropy coding algorithm in AVS video standard. Under the control of an embedded processor, the architecture can perform real-time entropy decoding for typical AVS HDTV sequences. Moreover, the architecture contains a pre-processing sub-module, which can support start code detection and de-stuffing

operation.

The research on the three key units of AVS video codec chip in this dissertation is helpful for the design of AVS SDTV/HDTV video codec chip and for the industrialization of AVS standard consequently.

Keywords AVS video codec; VLSI; motion estimation; loop filter; variable length code decoder